Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented). A process for producing a doping for a MOS transistor, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

after producing the doping, applying a layer selected from the group consisting of a polycrystalline layer and an amorphous layer to the surface;

performing a rapid thermal annealing process; and

subsequently carrying out a heat treatment step for producing an epitaxial layer and a buried doping for a MOS transistor.

Claims 2-3 (cancelled).

Claim 4 (currently amended). The process according to ~~claim 2~~ claim 1, which comprises forming the further amorphous layer to have a thickness of between 500 - 1000 nm.

Claim 5 (cancelled).

Claim 6 (previously presented). The process according to claim 1, which comprises carrying out the rapid thermal annealing process out at a temperature of between 1000° and 1100° C.

Claim 7 (previously presented). The process according to claim 1, which comprises carrying out the rapid thermal annealing process for a time period of between 10 and 60 seconds.

Claim 8 (original). The process according to claim 1, which comprises forming the semiconductor substrate from silicon.

Claim 9 (original). The process according to claim 1, which comprises forming the polycrystalline layer and the amorphous layer from silicon.

Claim 10 (original). The process according to claim 1, which comprises producing the doping by an ion implantation process.

Claim 11 (previously presented). The process according to claim 10, which comprises carrying out the ion implantation process using ions selected from the group consisting of B, P, As, In and Sb ions.

Claim 12 (previously presented). A process for producing a doping for a MOS transistor, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

after producing the doping, depositing a poly/α layer using a low-pressure and low-temperature chemical vapor deposition process to the surface of the semiconductor substrate; and

carrying out a heat treatment step for producing an epitaxial layer and a burled doping for a MOS transistor.

Claim 13 (cancelled).

Claim 14 (previously presented). A process for producing a doping for a MOS transistor, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

after producing the doping, depositing a poly/α layer to a thickness between 20 nm to 40 nm using a low-pressure chemical vapor deposition process to the surface of the semiconductor substrate; and

carrying out a heat treatment step for producing an epitaxial layer and a buried doping for a MOS transistor.

Claim 15 (previously presented). The process according to claim 12, which comprises carrying out a crystallization of the poly/α layer by performing a low-temperature step.

Claim 16 (original). The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of between 600° C to 700° C.

Claim 17 (original). The process according to claim 15, which comprises carrying out a wet etching operation out after performing the low-temperature step.

Claim 18 (original). The process according to claim 15, which comprises performing the crystallization at a same time as a formation of a gate oxide.

Claim 19 (original). The process according to claim 12, which comprises depositing the poly/α layer at a temperature of between 500° C and 600° C.

Claim 20 (original). The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of 650° C.

Claim 21 (previously presented): A process for producing a MOS transistor with a buried doping, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

after producing the doping, applying a layer selected from the group consisting of a polycrystalline layer and an amorphous layer to the surface;

subjecting the assembly to ion bombardment or to RTA processing with a rapid heat treatment to thereby destroy an oxide layer present between the semiconductor substrate and the polycrystalline or amorphous layer; and

subjecting the assembly to a heat treatment step for producing a monocrystalline layer and a buried doping from the layers and the semiconductor substrate for forming the MOS transistor.